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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,762	09/17/2003	Steven Woo	RAMB-01012US0	4148

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EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,762	WOO ET AL.	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 are pending for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1-4, 13-29 are rejected under 35 U.S.C. 102(a) as being anticipated by Kareenahalli et al. US 2004009850.

4. As per claim 1, Kareenahalli et al. disclose a method, comprising the step of:

initializing the system parameter [502 fig. 5; paragraph 0023, 0045, 0057];

operating a processing device responsive to the system parameter [paragraph 0002, 0003, 0048-0050];

comparing the operation value to a threshold value [paragraph 0013, 0058]; and

adjusting the system parameter responsive to the comparing step [paragraph 0013, 0063].

5. As per claim 2, Kareenahalli et al. disclose the system parameter is a page closing time stored in a memory controller [206 fig. 2; paragraph 0002].

6. As per claim 3, Kareenahalli et al. disclose the obtaining step includes determining a difference between page hits and page misses during a period of time [claim 1; paragraph 0052].

7. As per claim 4, Kareenahalli et al. disclose a first counter capable to obtain a number of page hits and a second counter capable to obtain a number of page misses [paragraph 0012] and comparator logic capable to output a parameter adjust signal responsive to the difference and the threshold value [512, 514 fig. 5].

8. As per claim 5, Kareenahalli et al. disclose the initializing step is performed by a BIOS software component [paragraph 0004, 0052].

9. As per claim 13, Kareenahalli et al. disclose

a first counter capable to output a number of page misses during a period of time;

a second counter capable to output a number of page hits during the period of time [paragraph 0029];

and, a comparator logic, coupled to the first and second counters, capable to output an adjust signal responsive to a comparison of a difference between the number of page hits and page misses to a threshold value [inherent from paragraph 0052-0056].

10. As per claim 14, Kareenahalli et al. disclose adjust signal increments a page closing time value [paragraph 0054, 0056 – zero, middle or infinite depended on the result of the comparison].

11. As per claim 15, Kareenahalli et al. disclose adjust signal decrements a page closing time value [paragraph 0054, 0056].

12. As per claim 16, Kareenahalli et al. disclose an average memory access time is decreased [inherent].

13. As per claim 17, Kareenahalli et al. disclose power consumption is decrease [inherent].

14. As per claim 18, Kareenahalli et al. disclose a BIOS software component initialized the period of time and the threshold value [paragraph 0029, 0045, 0052].

15. As per claim 19, Kareenahalli et al. disclose the adjust signal adjusts a page closing time value stored in a memory controller [202 fig. 2];

16. As per claim 20, Kareenahalli et al. disclose the device is a memory controller [paragraph 0022, 0030].

17. As per claim 21, Kareenahalli et al. disclose the device is coupled to a memory module [fig. 1, 2].

18. As per claim 22, Kareenahalli et al. disclose

a master device capable to retrieve data responsive to a page close time value [110 fig. 1; 202 fig. 2], including,

a first counter capable to output a number of page misses during a period of time;

a second counter capable to output a number of page hits during the period of time [paragraph 0029];

a comparator logic, coupled to the first and second counters, capable to output an adjust signal responsive to a comparison of a difference between the number of page hits and page misses to a threshold value [paragraph 0012, 0051], wherein the adjust signal adjusts the page close time value [paragraph 0030, 0053, 0055-0056; claim 1, 7]; and,

a memory device [104 fig. 1] , coupled to the master device, to provide the data.

19. As per claim 23, Kareenahalli et al. disclose the threshold value and the period of time is initialized by a BIOS software component [paragraph , 0004, 0012].

20. As per claim 24, Kareenahalli et al. disclose the master device is a memory controller [202 fig. 2].

21. As per claim 25, Kareenahalli et al. disclose the master device is a processor [102 fig. 1 – design choice].

22. As per claim 26, Kareenahalli et al. disclose the memory device is a Dynamic Random Access Memory ("DRAM") device [paragraph 0015].

23. As per claim 27, Kareenahalli et al. disclose the memory device is included in a memory module [inherent].

24. As per claim 28, Kareenahalli et al. teach the method and system for dynamically adjusts the page close time value of a memory device. Therefore, Kareenahalli et al. teach an article of manufacture to perform the method.

25. As per claim 29, Kareenahalli et al. disclose a memory capable of storing a page closing time value [202 fig. 2]; and

means [BIOS paragraph 0052] for adjusting the page closing time value responsive to an operation value.

26. Claims 8 –12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kahn et al. U.S. Patent 6,799,241.

27. As per claim 8, Kahn et al. disclose counting a number of page hits during a period of time;

counting a number of page misses during the period of time;

comparing the number of page hits to the number of page misses; and,

adjusting a page closing time value responsive to the comparing step [claim 1].

28. As per claim 9, Kahn et al. teach increasing the page closing time value responsive to the comparing step [claim 4].

29. As per claim 10, Kahn et al. teach decreasing the page closing time value responsive to the comparing step [claim 4].

30. As per claim 11, Kahn et al. teach the number of page hits is greater than the number of page misses [claim 4].

31. As per claim 12, Kahn et al. teach the number of page hits is less than the number of page misses [claim 4].

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kareenahalli et al. as applied to claim 1 above, and further in view of Williams U.S. Patent 5,774,704.

34. As per claim 6, Kareenahalli et al. teach the system parameter is the memory closing time. However, Kareenahalli et al. do not teach the system parameter is a processor operating frequency.

William teaches another computer system having a cpu, a device for dynamic cpu clock adjustment. The device is comprised a clock pulse generator for generating a clock frequency wherein the clock frequency is coupled to the cpu and is used by the cpu to synchronize and pace its internal operation. Specifically, William teaches the initializing of the processor operating frequency [502 fig. 5A] and subsequently adjusting the clock frequency according to the cpu load.

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Kareenahalli et al. with the system parameter as a processor operating frequency of William in order to avoid over heating of the cpu and/or other associated problems such as excessive power consumption [col. 2 lines 60-64].

35. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kareenahalli et al. as applied to claim 1 above, and further in view of Crocker et al. U.S. Patent 5,915,265.

36. As per claim 7, Kareenahalli et al. teach the system parameter is the memory closing time. However, Kareenahalli et al. do not teach the system parameter is a number of memory devices in a memory module operating in a particular mode.

Crocker et al. teach a method and system for dynamically sizing a dedicated memory in a shared memory buffer architecture. Specifically, Crocker et al. teach at initial boot, system BIOS programs control register to allocate a dedicated number of memory devices in a memory module in response to the performance requirements [abs]. If after initial boot, the performance requirements change, it may necessitate a change in dedicated number of memory devices.

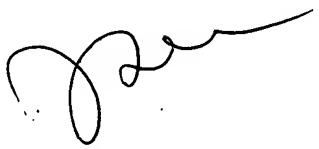
At the time of the invention was made, it would have been obvious to one of ordinary skill in the art the have modified the system of Kareenahalli et al. with system parameter as a number of memory devices operating in a particular mode of operation as taught by Crocker et al. in order to avoid excessive power consumption.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Vincent Tran